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12EC027

M.Tech. Degree Examination, June/July 2013
Design of VLSI Systems

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Discuss hierarchy, regularity, modulatiry and locality, with one example each. **(08 Marks)**

b. Explain the different general purpose programmable devices. **(08 Marks)**

c. Write the diagrams of Actel and quicklogic cells. **(04 Marks)**

2 a. Explain SOG in brief, and list the factors to keep the cost low. **(08 Marks)**

b. What is logic optimization? Explain with a typical flow diagram. **(08 Marks)**

c. What is network isomorphism? Explain in detail. **(04 Marks)**

3 a. Write and explain the circuit diagram of a 4-bit carry-ripple adder with PG logic. **(06 Marks)**

b. Write the schematic diagram of the 4-bit unsigned array multiplier. **(08 Marks)**

c. Along with the tabular column, explain the modified booth encoding procedure. **(06 Marks)**

4 a. Discuss the working of 6T – SRAM along, with a neat diagram. **(04 Marks)**

b. Write the circuit diagram of clocked sense amplifier, and explain its operation. **(06 Marks)**

c. Draw the basic ROM architecture using NOR array and explain its working. **(04 Marks)**

d. Draw and explain the 4 × 4 CAM array. Give an application of CAM. **(06 Marks)**

5 a. What is an FSM? Explain its types with figures. Why is FSM necessary in the design of control subsystems? **(06 Marks)**

b. Obtain the PLA implementation of the following expressions :

$Z_0 = x_0 + \bar{x}_1$

$Z_1 = x_1 + (x_0 \cdot \bar{x}_2)$

$Z_2 = \bar{x}_0 \cdot \bar{x}_1 \cdot x_2$

$Z_3 = (x_0 \cdot \bar{x}_1 \cdot \bar{x}_2) + (\bar{x}_0 \cdot \bar{x}_1 x_2)$ **(04 Marks)**

c. What are the properties of I/O subsystems? Explain the basic I/O pad circuits. **(10 Marks)**

6 a. Estimate the peak current and the power requirement for a chip with 20 K registers, if T_{clock} = 10 ns, and $T_{rise/fall}$ = 1 ns. The chip operates from 5V supply, and the capacitance per bit is 0.1 pF. **(10 Marks)**

b. Explain the generation of global clock with respect to PLL, with block diagram as well as circuit diagram. **(10 Marks)**

7 a. Explain the Non – recurring engineering costs. **(06 Marks)**

b. Write the formula for the recurring costs, with complete details. **(04 Marks)**

c. What is boundary scan? Explain along with the TAP architecture. **(10 Marks)**

8 Write short notes on :

a. Stuck – at faults

b. Observability

c. Controllability

d. IDDQ testing. **(20 Marks)**

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